**Abstract**

Spin Transfer Torque Random Access Memory (STT-RAM) is a promising technology for information storage in the form of magnetic field rather than existing charge-based memories like static random-access memory (SRAM), dynamic random-access memory (DRAM) and flash. Charge-based memory is notorious for its volatility and constant power usage. STT-RAM technology is advantageous for its non-volatility, complementary metal-oxide semiconductor (CMOS) compatibility, programmability and hardware security through lookup tables (LUTs). The contents of LUTs may be programmed and simulated in a software called Synopsys to implement any arbitrary logic function. Due to circuit complexity, LUTs occupy significantly more area than logic gates, so the delay and power consumption inevitably increase. The 4-bit adder 74283 benchmark circuit was chosen as the case study for this project. The purpose of this project is to maximize the number of LUTs implemented while minimizing delay and power consumption by replacing specific gates with LUTs. The logic gates of the 4-bit adder were individually mapped with LUTs, and then the delay, active power, standby power, power delay product (PDP) and area were measured. From the extracted data, we found that certain gates produced higher delay and power consumption but the majority of mapped gates do not have delay penalties. Next, three mapping optimization methods — dependent, independent and parametric-aware selection — were used to map certain set of gates with their respective LUTs. The results provided tremendous insight on which set of gate selections are best to map in order to increase hardware reconfigurability and security, which is the trend of STT-LUT applications. Using the optimal pathway, STT-LUT implementation can achieve maximum efficiency with a mix of complex logic gates, which means faster processing of reconfigurable hardware such as Field Programmable Gate Arrays (FPGA). This implementation provides less power leakage and usage, and ease of reconfigurable non-volatile hardware.